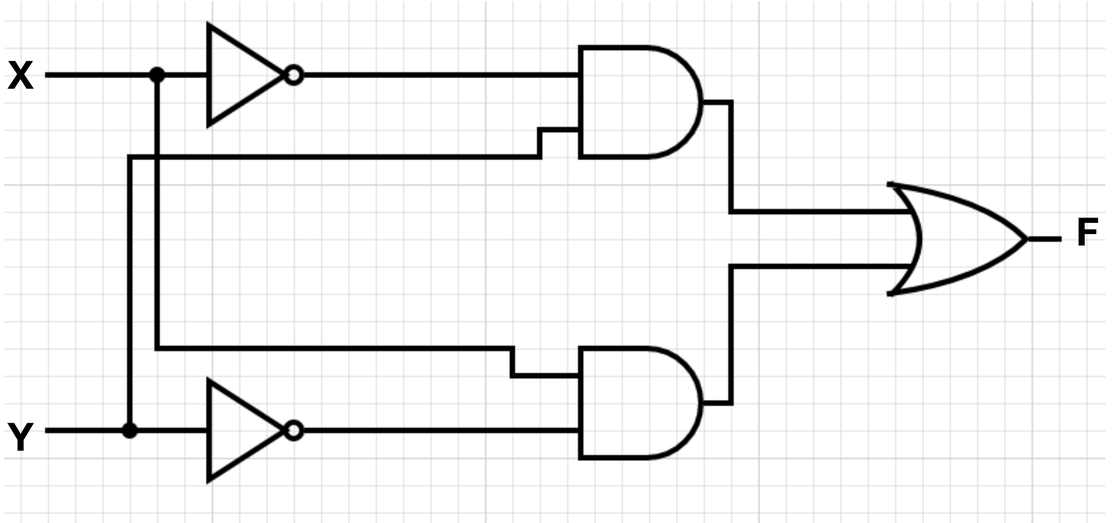
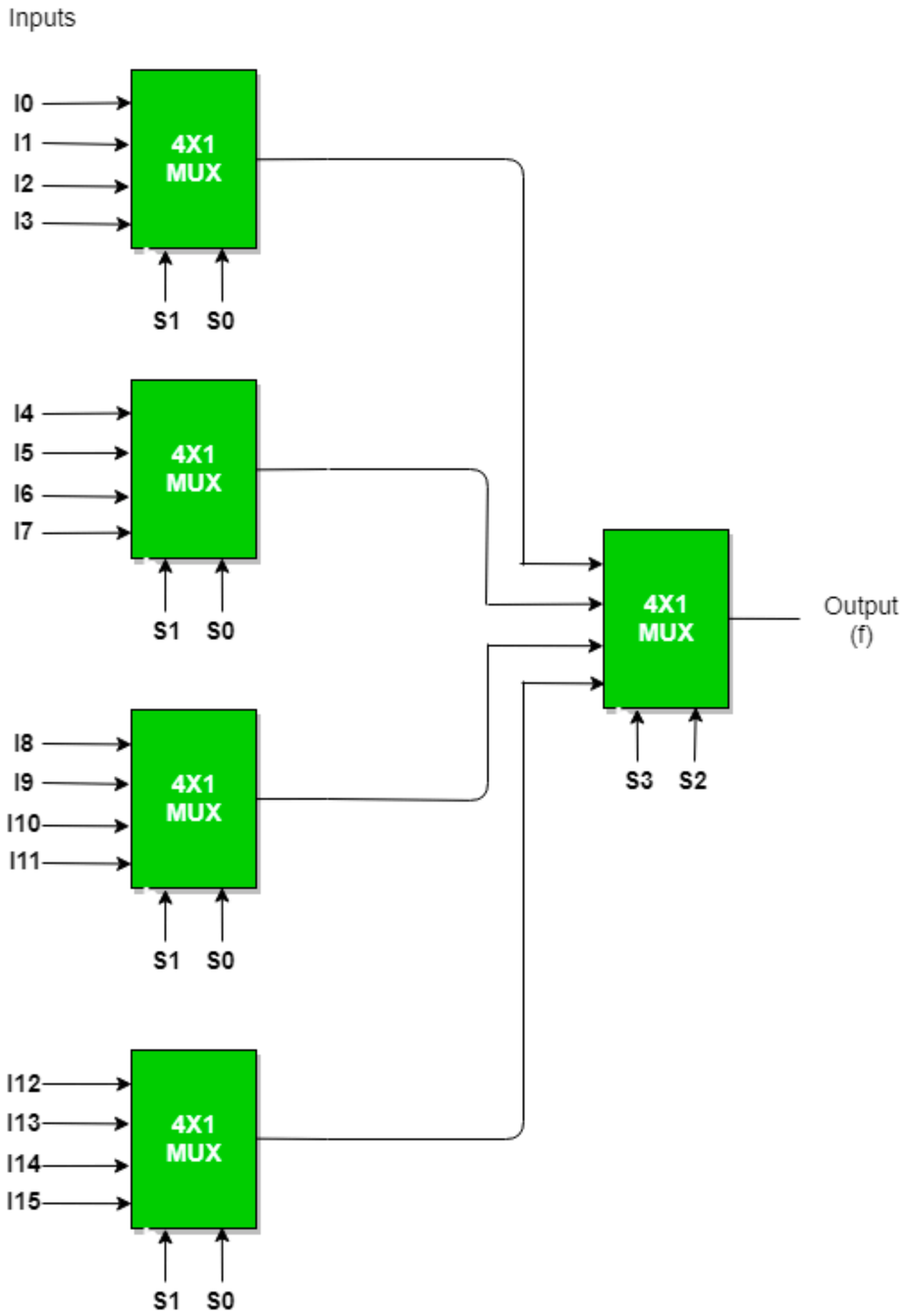
TUTORIAL-2

Q-1- Which of the following logic gate is represented by the following logic circuit ?

A-NAND
B-NOR
C-XOR
D-XNOR



Q-2- CONSTRUCT 16:1 MUX USING 4:1 MUX ONLY.


Inputs
I0
I1
I2
I3
4X1
MUX
S1
S0
I4
I5
I6
I7
4X1
MUX
S1
S0
I8
I9
I10
I11
4X1
MUX
S1
S0
I12
I13
I14
I15
4X1
MUX
S1
S0
4X1
MUX
S3
S2
Output
(f)

How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

(A) 7

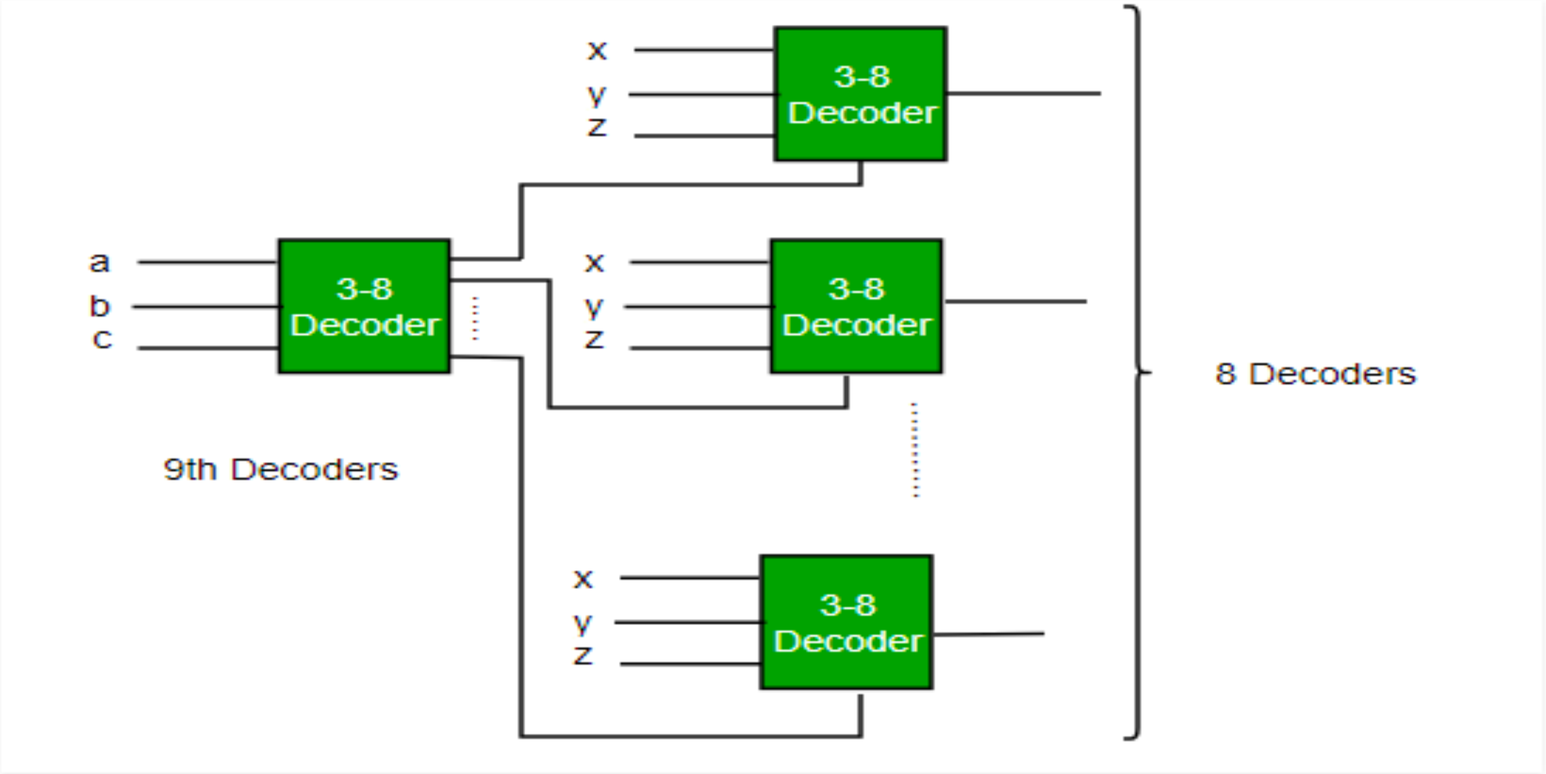
(B) 8

(C) 9

(D) 10

Answer: (C)

Explanation:



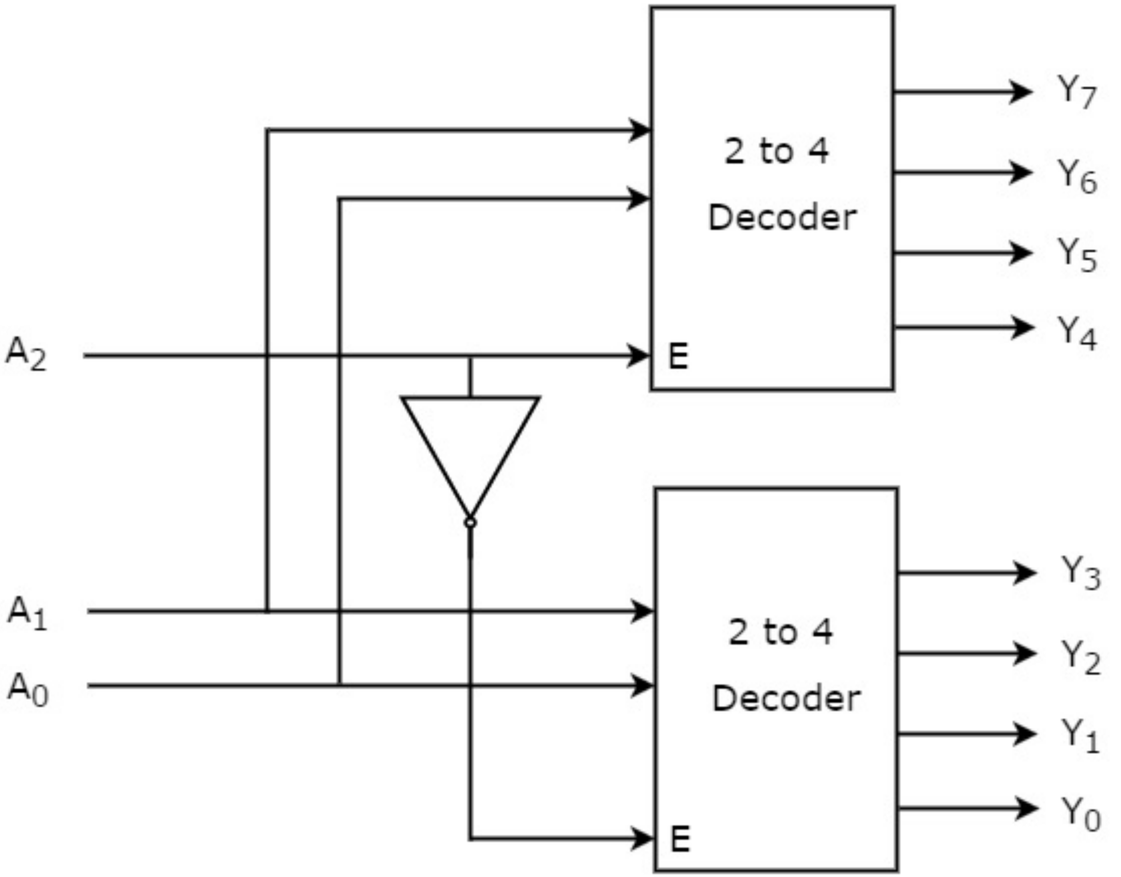
So total signals in=a, b, c, x, y, z i.e. 6

And total output =8*8=64

hence required decoders (from fig.) = 9 so ans is (C) part.

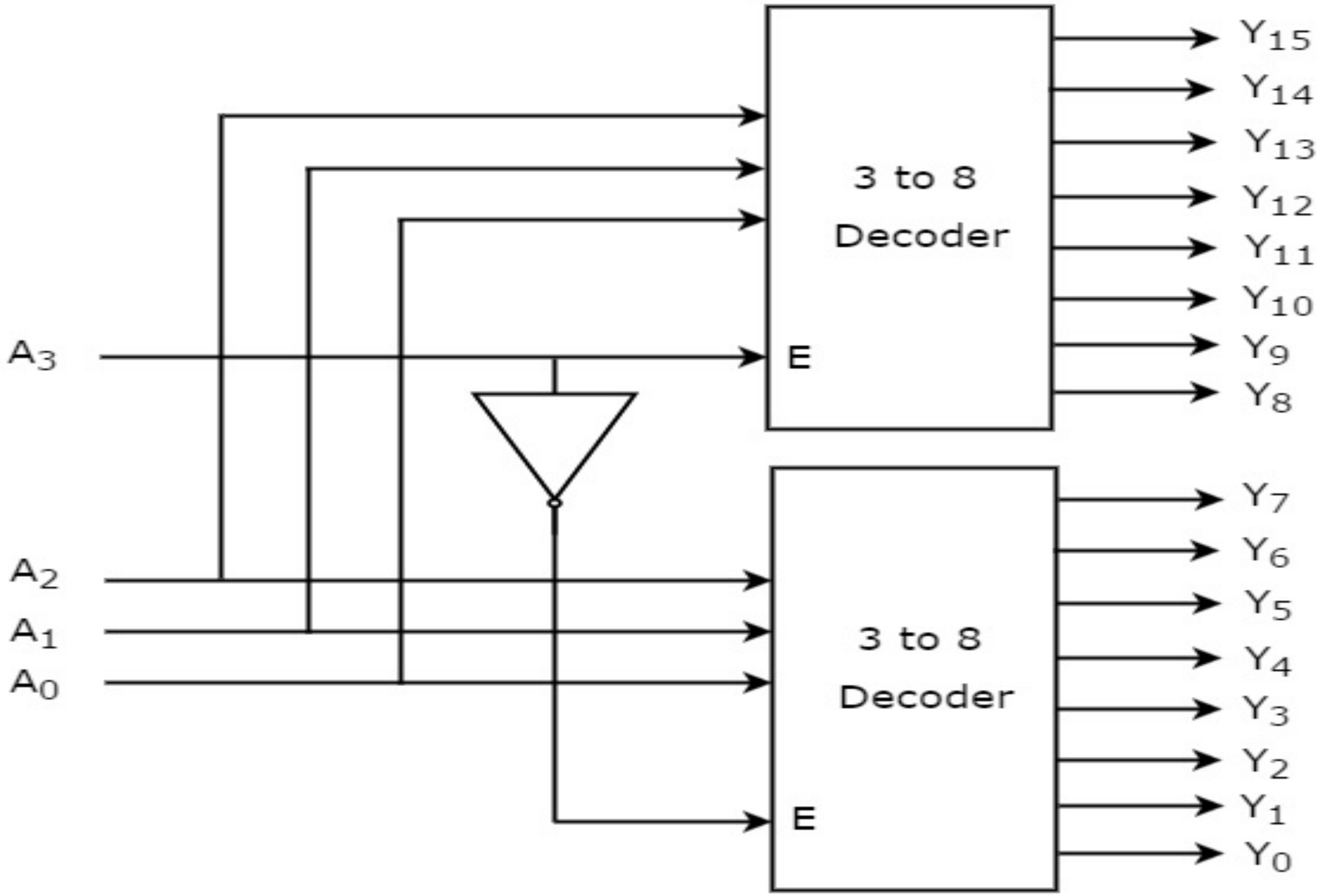
Q- CONSTRUCT DECODER WITH SIZE 3:8 USING TWO 2:4 DECODERS

Therefore, we require two 2 to 4 decoders for implementing one 3 to 8 decoder. The **block diagram** of 3 to 8 decoder using 2 to 4 decoders is shown in the following figure.



Q- CONSTRUCT DECODER WITH SIZE 4:16 USING TWO 3:8 DECODERS

Therefore, we require two 3 to 8 decoders for implementing one 4 to 16 decoder. The **block diagram** of 4 to 16 decoder using 3 to 8 decoders is shown in the following figure.



Connecting Registers - Bus Transfer

- For a bus system to multiplex k registers of n bits each
  - No. of multiplexer = n = No. of bits
  - Size of each multiplexer = k x 1, k data lines in each MUX

- **Construction of bus system for 8 register with 16 bits**
  - **16 bit register X 8**
  - **16 MUX 8X1 multiplexer—— NO OF MUX REQUIRED**
  - **Bus selection S0, S1, S2**